

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated August 24, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due consideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 2-6 and 12 are under consideration in this application. Claims 1 and 7-11 are being cancelled without prejudice or disclaimer. Claims 2-6 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention. A new claim 12 is being added to recite another embodiment described in the specification.

All the amendments to the claims are supported by the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

Claim 6 was objected to due to informalities, and the Examiner has requested correction thereof. As indicated, the claims are being amended as suggested by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Allowable Subject Matter

Claim 6 would be allowed if it is rewritten in independent form to include the limitations of the base claim and any intervening claims.

As claim 6 is being corrected as suggested by the examiner and rewritten into independent form to include the limitations of the base claim and any intervening claims, it is in condition for allowance.

Prior Art Rejections

Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by US Pat. App. Pub. No. 2004/0201729 of Poplin et al. (hereinafter "Poplin"), claims 2-5 were rejected as being anticipated by US Patent No. 6,710,818 to Kasahara et al. (hereinafter "Kasahara"), and

claims 7-9 and 11 were rejected as being anticipated by US Patent No. 6,882,363 to Oda et al. (hereinafter "Oda"). Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Oda in view of US Patent No. 6,900,837 to Muramatsu et al. (hereinafter "Muramatsu"). The prior art references of Chung et al. (6,271,884) and Toyoda et al. (6,630,953) were cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed.

As claims 1 and 7-11 are being cancelled without prejudice or disclaimer, the relevant rejections thus become moot.

The imaging system including a solid-state CMOS imaging device 10 and a signal processing semiconductor integrated circuit 20 for processing read-out signals of pixels 110 from said solid-state CMOS imaging device 10 of the invention (for example, the embodiment depicted in Figs. 1 and 12; p. 30, 2nd paragraph; p. 31, 2nd paragraph), as now recited in claim 2, comprises: first level detection means 24b which detects brightness on a first area shown in Fig. 12b (32 pixels * 1 line) set up on an imaging area of said solid-state CMOS imaging device, the first area which is predetermined area in a frame; second level detection means 24a which detects brightness on a second area shown in Fig. 12a (192 pixels * 96 lines) which is set up on an imaging area of said solid-state CMOS imaging device 10, and is larger than said first area, the second area which is a predetermined area in the frame; and judgment means which judges turning-on-and-off of a light source illuminating in accordance with an object to be imaged on the basis of detection levels of said first and second level detection means 24b, 24a.

As the first and second areas which are predetermined areas in a frame, the invention can distinguish clearly from changes in photographic surroundings of the object and detect variation in the turning-on-and-off of the illumination light source by the first and second detection means (p. 39, lines 3-11).

Applicants respectfully contend that Kasahara fails to teach or suggest such "first and second areas which are predetermined areas in a frame" as in the invention.

In contrast, the averaging circuit 3 of Kasahara's imaging system averages data (SUM_{n-1,i} SUM_{n-2,i} SUM_{n-3,i}) that correspond to the ith line at frames n-1 to n-3 (col. 8, lines 41-45) to define the first and second areas such that the first and second areas vary along with the data, rather than being predetermined areas in a frame as in the invention.

Kasahara fails to teach or suggest each and every feature of the present invention as recited in the independent claim 2. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The

withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

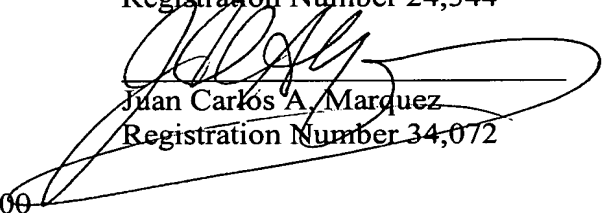
Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

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